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Qualification of a spin apply, photodefinable polymer for

packaging of automotive circuits

OVERVIEW Spin apply polymer coatings can be used in packaging applications as a stress buffer passivation layer for improved device reliability. They can also serve as dielectric and passivation layers in bond pad redistribution circuits for flip-chip packaging. A high T_g, photodefinable polyimide was selected for both applications, due to good chemical resistance and desirable adhesion characteristics to silicon nitride, various molding compounds, aluminum, and to itself. The product exhibited a wide process window, and tapered via slopes were obtained for metallization through minor process modifications.

An increasing variety of automotive applications from engine control modules to antilock braking systems and more sophisticated vehicle roadside communication devices are using ICs. Producers of automotive semiconductor devices must face the continuing challenge of increasing circuit density, reducing costs, and improving the reliability of devices, all of which must perform consistently under harsh environmental conditions.

Automotive electronics companies are evaluating spin apply polymer coatings as secondary passivation layers for improved device reliability and as dielectric layers for flip-chip packaging configurations to increase device packaging density. This study involving eight different spin apply polymers focuses on an effort to qualify a polymer technology for both application areas.

Stress buffer passivation

To keep production costs down, most automotive circuits are packaged in nonhermetic plastic molding compounds. Two reliability problems can occur with this packaging configuration for large die and devices that can be subjected to thermal stress or shock during their operation. The first concerns stresses induced by the molding compound, which can lead to cracking of the device passivation or metallization layers. A typical source is the difference between the coefficient of thermal expansion (CTE) of the molding compound and the silicon chip. The inherent abrasiveness of the inorganic molding compound fillers, which can damage the thin films on the surface of the chip, further complicates the problem. Reliability also suffers when the molding compound delaminates from the surface of the IC, creating a void where moisture can permeate and ultimately lead to corrosion and device failure (Fig. 1).

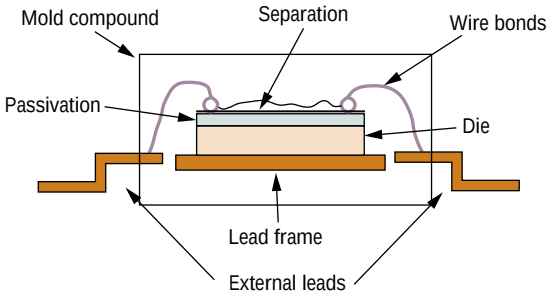

Figure 1. Schematic of a plastic-molded IC.

To address the problem of stress-induced die cracking and molding compound delamination, a thick, polymeric, secondary passivation layer or "stress buffer passivation" (SBP) layer applied over the primary silicon nitride passivation layer can cushion the device from molding compound stresses and abrasive fillers, thus improving device reliability [1].

Polyimide-based materials have historically been used for SBP layers due to relatively low stress levels, proven chemical resistance, and good thermal and mechanical stability [2]. In recent years, producers have made self-imaging or photodefinable versions of these materials to simplify the patterning sequence, lower the number of processing steps, and improve yields. These coatings are typically applied at the wafer level, usually as one of the last processing steps in the fab. The improved resolution provided by a photodefinable polyimide, combined with inherently good dry etch chemical resistance [1], permits the SBP layer to double as a dry etch mask for patterning the primary silicon nitride passivation layer. In this case, the SBP layer allows the fab to eliminate a photomask step.

The study discussed here evaluated two photodefinable polyimide products for their effectiveness as a spin apply SBP layer on test circuits packaged with two different kinds of molding compound. An established, negative-tone, photodefinable polyimide (PI-2771) that can be developed with either solvent or aqueous developers was compared to a newer, negative-tone, photodefinable polyimide that featured a glass transition temperature (T_g) of 350°C. The new product, HD-4000, could potentially be used for other higher-temperature dielectric layer applications. In contrast to the incumbent product, it showed improved resolution and no haze. Figure 2 shows patterned cured films of both stress buffer layers.

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Mold compound adhesion tests were run on the two overcoat materials with two molding compounds. The tests examined the effect of a plasma de-scum processing step after polyimide cure as a process variable. After assembling parts into 28-lead SOIC packages with 300 units in each cell, a random sample of parts was checked for delamination using ultrasonic microscopy at two points: following the package assembly, and subsequent to an IR reflow. Table 1 summarizes the test results. Without the plasma de-scum step, delamination appeared in one of the mold compounds and the PI-2771 polyimide after initial packaging, and with the other mold compound after IR reflow. HD-4000 showed no failures in any of the test cells. The parts that went through plasma de-scum were subjected to JEDEC Level Two moisture conditioning and then an IR reflow. As shown in Table 2, none of the material sets displayed delamination after the completion of plasma de-scum on the cured polyimide.

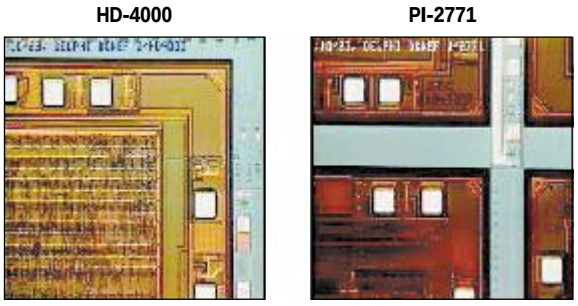

Figure 2. ICs with both cured polyimide films tested, HD-4000 and PI-2771.

Table 1. Initial inspection after package assembly and IR reflow

Wafer number	Polyimide type	Mold compound	De-scum?	Number tested	Delaminations after assembly	Delaminations after IR testing (235°C)
E6	PI-2771	Nitto	No	27	0	23
G6	PI-2771	Sumitomo	No	27	27	N/A
E2	PI-2771	Nitto	Yes	27	0	0
G0	PI-2771	Sumitomo	Yes	27	0	0
F4	HD-4000	Nitto	Yes	27	0	0
H2	HD-4000	Sumitomo	Yes	27	0	0
G5	HD-4000	Nitto	No	27	0	0
O5	HD-4000	Sumitomo	No	27	0	0

Interlayer dielectric material evaluation for flip-chip packaging

Current investigations are examining direct chip attach as a way to increase circuit density and signal speed in the design of automotive circuits. Conversion of conventional wire-bonded ICs to a flip-chip configuration through bond pad redistribution (BPR) is one avenue under investigation.

This conversion technique involves the redistribution of bond pads set around the perimeter of the IC, to solder bumps arranged across the entire top surface of the die [3]. Figure 3 shows a cross section of the construction of the bond pad rerouting structure. Bond pads are rerouted from the edge of the IC to solder balls positioned in a wider pitch across the center section of the chip. The following process flow was used to create the material stack in this construction: 1) application of a polymeric dielectric layer coated over the silicon nitride passivation layer; 2) deposition of thin-film runners and solder bump pads; 3) application of a polymeric passivation layer; 4) deposition of an under bump metallization (UBM); and 5) application of solder bumps for direct chip attach.

A spin apply polymeric layer was chosen as the dielectric and passivation layer for flip-chip packaging in place of traditional oxide deposition because these films can be applied in inherently thicker layers than oxides. They also have inherently higher elongation and a much lower modulus than traditional CVD layers. Finally, the polymer layers offer the potential to absorb the stresses that can occur during thermal excursions with differences in the coefficients of thermal expansion (CTE) that can exist between the silicon chip and various laminate or ceramic substrates.

With this design configuration, 4mil pitch wire bond pads could be readily repositioned over the die, resulting in a 16mil pitch (11.3mils diagonally) flip-chip design (Fig. 4a). Using these design rules, it was possible to achieve 220 bumps or I/Os on a 400mil square (4 × 4) die or 95 bumps on a 200mil square (2 × 2) die (Fig. 4b).

Seven different, spin apply, photodefinable polymers were evaluated for the dielectric and passivation layers in this application. This group of materials can be further subdivided into four different polymer groups: polyimide, benzocyclobutene (BCB), polynorbornene, and polybenzoxazole (PBO). Table 3 summarizes some of the associated cured film properties.

Table 2. After JEDEC Level Two moisture conditioning* and after IR reflow**

Wafer number	Polyimide type	Mold compound	De-scum?	Number tested	Delaminations after assembly	Delaminations after IR testing
E2	PI-2771	Nitto	Yes	108	0	0
G0	PI-2771	Sumitomo	Yes	108	0	0
F4	HD-4000	Nitto	Yes	108	0	0
H2	HD-4000	Sumitomo	Yes	108	0	0

*600 cycles, accelerated thermal cycling; **235°C

Performance criteria

Two performance criteria for the polymer layers were deemed necessary in the construction of the interconnect structure: 1) chemical resistance to the plating and cleaning solutions required for the stack construction (which could potentially be harsh on certain organic materials); and 2) adhesion to the nitride base, aluminum metallization, and UBM, as well as polymer-to-polymer intercoat adhesion.

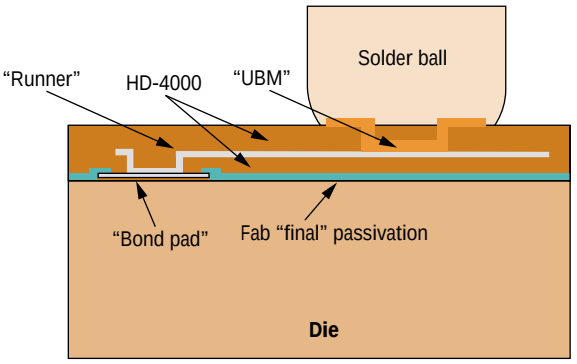

Figure 3. Cross-sectional view of the rerouting of the bond pads.

All seven polymers were evaluated against these two criteria for initial qualification. Subjecting cured polymer films to a series of chemicals specific to the process conditions in the fabrication of the BPR interconnect allowed for the measurement of the chemical resistance. The films were then checked for crazing or delamination to the substrate or delamination of overlying metallization and cover coat layers.

A standard bump-shear test measured the adhesion strength of solder balls to examine the overall integrity of the two-layered BPR construction. The measurement of the net shear force and analysis of the mode of failure were used to determine if the shearing occurred through the solder ball (preferred route), or if the mode of failure occurred at one of the metal-polymer or polymer-substrate interfaces (Table 3).

Chemical resistance test results

Based on this screening, chemical resistance surfaced as an issue with four of the seven material candidates. Some of these materials experienced problems with only the final chemical stripping solution, while others experienced problems with more than one of the chemicals associated with the base process.

Of the three polymers that passed the chemical resistance test, only one photodefinable polyimide (HD-4000) consistently passed the solder ball shear test without delamination at the bond pad metallization or silicon nitride interfaces. To further explore the potential of this material, four wafer-level builds were made with both 2 × 2 and 4 × 4 over a span of nine months. Initial fabrication of the test parts produced solder bumps of an average height of 5.1mm. Wafer yields were 99–100%, based on visual inspections for missing bumps, as well as metal and/or polyimide damage.

Bump-shear test results

Bump-shear tests on the solder bumps yielded an average of 61g at a shear rate of 4mm/sec, with all modes of failure being a shear through the solder ball. These results compare to a reading of 60–70g for a standard flip-chip solder ball of the same size. Using a higher shear rate of 19mm/sec resulted in an average of 69g, although approximately 10% of the failures occurred at the aluminum-polyimide interface versus through the solder ball. These measurements compare to a value of 70–80g at this rate for a standard flip-chip solder ball of the same size. Figure 5 shows examples of the failure mode. The real test of the BPR structure is making it through the stresses during the assembly to laminate substrates.

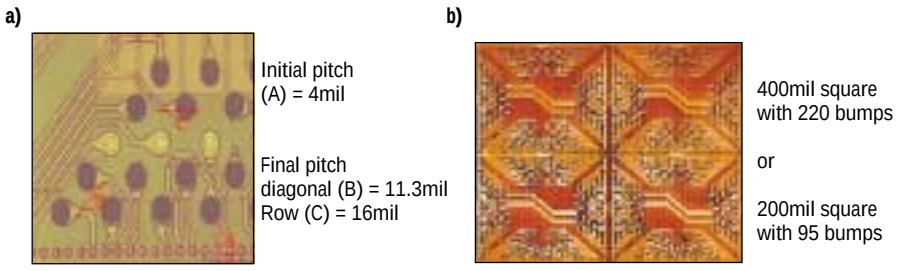

Figure 4. The test chip: **a)** rerouting design, and **b)** layout.

After completing assembly using die from the four wafer-level builds bonded to both laminate and ceramic substrates, a measurement of the daisy chain resistance yielded an average value of 33.5Ω for 2 × 2 die and about 66.3Ω for 4 × 4 die. These results indicated excellent solderability and no damage to the BPR structure. In the past, assembly of such BPR chips to laminate caused high resistance

Table 3. Polymer properties from published literature and Delphi test results

	BCB	Pre-imidized polyimide	Polynorbornene	Polyimide A	Polyimide B	PBO	Polyimide C
Moisture uptake (%)	<0.2	2	0.10	2	2	2	1.3
Tensile strength (Mpa)	87	97	NA*	>120	200	100	170
Modulus (Gpa)	2.9	3.2	NA	NA	3.5	2.5	2.9
Elongation (%)	9	8	20	>50	45	65	73
CTE (ppm/°C)	52	24	80	50	30	55	27
Dielectric constant	2.65	2.8	2.5	3.4	3.0	2.9	3.3
Chemical resistance	Excellent	Poor	Poor	Excellent	Excellent	Moderate**	Moderate
Shears	Nitride	NA	NA	Nitride	Solder	NA	NA

*not available; **resistant to every chemical except final strip solutions

due to degradation of the BPR structure.

The aspect ratio of the photodefinable polyimide selected exceeded 1:1 in 5µm cured films, which was more than adequate for the design rules of this circuit. The wall slope of the patterned vias in the dielectric layer, however, is critical to successful metallization coverage. To image these builds with a contact/proximity printer, the gap between the polyimide layer and the printer photomask was varied from contact (25µm) to 75µm. A gap of 30–75µm that produced a wall slope of about 50° with minimal crowning was found adequate for good intermetal contact. This allowed for a much larger process window when compared to earlier photodefinable polymers tested.

Figure 5. Bump shear failure modes.

Figures 6a and 6b show two cross sections of the completed BPR circuits. As shown in the cross section of the completed circuit bonded to a laminate substrate (Fig. 6a), the planarization capability of the polyimide dielectric layer was adequate for this application and can be seen over the circuit topography of the test chip. (The figure also shows the solder ball interface to the die and the motherboard). Figure 6b shows the redistribution layer runner, UBM, patterned layers of the photosensitive polyimide dielectric and passivation layers, and the tapered wall slope of the passivation layer.

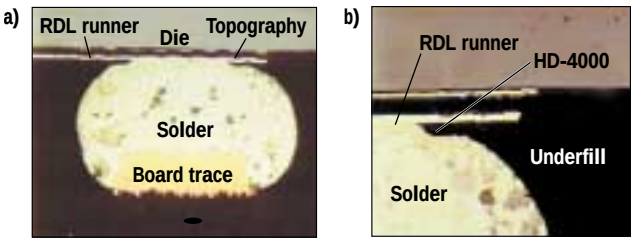

Figure 6. Cross sections showing **a)** chip assembled to laminate board, and **b)** redistribution structure.

Final qualification of the new BPR interconnect scheme will involve a series of thermal shock, thermal cycling, and high-temperature storage stress tests required for automotive IC applications. These tests are currently in process.

Conclusion

With the qualification of a new, high-T_g, photodefinable polyimide, Delphi Delco can now use the same base material in stress buffer passivation layers and bond pad redistribution circuits for flip-chip design. The wider process windows, good chemical resistance, and desirable adhesion characteristics of the material should help automotive electronics manufacturers achieve the goals of increased device reliability and higher packaging density. It should be noted that the test results reported were for polymeric materials available at the time of the evaluation, which spanned a period of 18 months. It is possible that newer versions of these materials would show improved performance under the same test conditions in a similar set of evaluations. ■

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